

REMARKS

In the non-final 10 March 2006 *Office Action*, the Examiner rejects Claims 1-20. Applicants thank the Examiner with appreciation for the careful consideration and examination. No new matter is believed introduced into the Application by this submission.

After entry of this Response, Claims 1-20 are pending in the Application. Applicants respectfully assert that Claims 1-20 are in condition for allowance and respectfully requests reconsideration of the claims in light of the following remarks. Applicants believe that Claims 1-20 are allowable for the following reasons.

I. Claim Objections

The Examiner objected to several of Applicants' claims (Claims 1, 2, 4, 6, 8, 12, 17, and 20). The Examiner also suggested amendments to overcome the objections and Applicants thank the Examiner for the suggestions. Applicant incorporates these suggestions in the above-presented amendments and respectfully asserts that the objections are overcome. Withdrawal of the claim objections is respectfully requested.

II. 35 U.S.C. § 101 Rejection

The Examiner rejects Claims 2-3 under § 101 asserting that the claimed invention is directed to non-statutory subject matter. Applicants amend Claims 2-3 such that they are now directed to a single statutory invention class. Accordingly, Claims 2-3 overcome the § 101 rejection. Withdrawal of the § 101 rejection is respectfully requested.

III. 35 U.S.C. § 112 Rejection

The Examiner rejects Claims 2-3 and 11-16 under § 112 asserting that these claims are indefinite. Applicants amend Claims 2-3 such that they are now directed to a single statutory invention class. The Examiner also suggested amendments to overcome the § 112 rejections and Applicants thank the Examiner for the suggestions. Applicant incorporates these suggestions in the above-presented amendments and respectfully asserts that the rejections are overcome. As for the claimed "the command tenure" in Claim 13, Applicant notes that Claim 11 does recite "a command tenure" thereby providing appropriate antecedent basis for Claim 13's recitation of "the command tenure". Withdrawal of the § 112 rejection is respectfully requested.

IV. The Pending Claims and the 35 U.S.C. 103 Rejections

The Examiner rejects Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over *Gustavson* (USPN 6,442,644) in view of *Olarig* (USPN 6,134,638). The Examiner asserts that the *Gustavson-Olarig* combination discloses the subject matter contained in Claims 1-20.

Applicant respectfully traverses the § 103 rejection.

As the Examiner will recall, Applicants' claimed invention is directed toward a memory system that can operatively coordinate memory transactions based on rank specific memory timing adjustments. Indeed, Applicants' claimed invention utilizes two parameters to adjust memory transaction timing parameters in certain embodiments (see claims for exact claim language). A whole number portion is used to make gross adjustment to timing parameters, and a fractional portion is used to make fine adjustments to the timing parameters. Thus, Applicants' claimed invention implements a double adjustment to memory transaction timing parameters according to certain embodiments. The double adjustment enables Applicants' claimed invention to make rank-specific adjustments for a memory transaction timing parameter of a memory component to improve bus timing margins.

In contrast, the cited combination does not teach or disclose a system utilizing a double adjustment. Rather, the cited combination combines two single adjustment systems that does not render Applicants' claimed invention unpatentable. Applicants have meticulously reviewed the references cited by the Examiner and can not find any teachings of a double adjustment system as claimed by Applicants. Applicants therefore respectfully assert that Applicants' claimed invention of Claims 1-20 is patentable over the cited combination.

Applicants also respectfully assert that Claims 1-20 are allowable over the cited combination for additional reasons, including that a *prima facie* case of obviousness has not been set forth. As MPEP § 2143 provides, a *prima facie* case of obviousness requires three findings. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations as a whole as required by 35 U.S.C. § 103. See MPEP § 2142 & § 2143.

Applicant respectfully asserts that the cited combination does not teach each and every claimed element and limitation of Claims 1-20. For example, the Examiner asserts that

Gustavson teaches “a table comprising at first timing adjustment signal associated with a rank of a memory component and a second timing adjustment signal associated with the memory component” as recited in Claim 1 when discussing latency values for IAMUs. Applicant respectfully submits that *Gustavson*’s reference to latency values are not timing adjustment signals. Rather, these latency values only represent data about IAMUs and are not timing adjustment signals. Indeed, *Gustavson* does not use the latency values as timing adjustment signals; therefore, *Gustavson* does not teach this element of Claim 1. Moreover, *Gustavson* fails to teach timing adjustment signals stored in a look up table as claimed by Applicants. Similarly, Applicant respectfully submits that *Gustavson* fails to teach each and every claimed element and limitation as recited in Claims 11 and 17.

Gustavson also fails to teach additional claimed elements and limitations. For example, *Gustavson* fails to teach “calculating a rank of the DDR memory component from a command tenure” as recited in Claim 11. Indeed, the portion of *Gustavson* cited by the Examiner as teaching this claimed feature fails to fairly suggest that *Gustavson* calculates any information about a memory component. While *Gustavson* may teach to obtain information about IAMUs, such teaching does not teach to calculate a rank of a memory component from a command tenure as claimed by Applicants.

Applicants also respectfully assert that *Olarig* fails to teach or disclose any portion of Applicants’ currently claimed invention. For example, *Olarig* fails to teach or suggest a memory cell that further adjusts a data strobe signal using a second portion of a timing adjustment signal by an amount less than an associated first portion as recited in Claim 1 (see Claim 1 for specific claim language). Indeed, *Olarig* does not even teach Applicants’ claimed memory cell, thus *Olarig* necessarily fails to teach a memory cell having Applicants’ claimed features.

In addition, *Olarig* fails to teach any claimed element or limitation of Claims 11 or 17. For example, *Olarig* does not teach or fairly suggest “extracting at least one timing adjustment signal from a look-up table with the calculated rank” as asserted by the Examiner. It is important to note that *Olarig* (or *Gustavson*) does not teach to calculate anything thereby preventing the cited combination from extracting data based on a calculated rank. Similarly, with regard to Claim 17, *Olarig* (and *Gustavson*) does not teach or fairly suggest a delay clock circuit having certain features as Applicants claims. The portions of *Olarig* cited by the Examiner do not teach such a feature; rather, they merely teach to provide a certain clock frequency to a memory

component. Such teaching, however, fails to teach what Applicants claims in Claim 17.

Applicants also respectfully assert that the cited combination is improper and can not support a proper § 103 rejection. More specifically, Applicants respectfully assert that *Gustavson* would not work properly function if modified with *Olarig*. As the Examiner knows, a combination is not proper if the references would not function properly as intended. MPEP § 2143.01, Section V. If *Olarig* was combined with *Gustavson*, the buffers and queues of *Olarig* would render *Gustavson* unsatisfactory for its intended purpose. For example, *Olarig*'s buffers and queues would not allow *Gustavson* to adequately initialize and calibrate memory modules since such initialization and calibration signals would get bogged down in *Olarig*'s buffers. (See e.g., *Olarig*, Figures 2-3, 5; c. 4, ll. 38-55; c. 5, l. 20 – c. 7, l. 16; c. 8, l. 45 – c. 9, l. 23). Further, *Olarig* is not properly combinable with *Gustavson* since *Olarig*'s system can not function properly without its buffers as the buffers are essential to *Olarig*'s functionality. *Id.*

In addition, a reasonable expectation of success must be set forth as part of a prima facie case of obviousness. Because the cited combination would force *Gustavson* and *Olarig* to function improperly, a reasonable expectation of success that Applicant's claimed invention would result from the cited combination can not be provided. Thus, *Olarig* can not be combined with *Gustavson*.

For at least these reasons, Applicant respectfully submits that Claims 1-20 are allowable over the references of record. Withdrawal of the § 103 rejection to Claims 1-20 is respectfully requested.

V. Fees

Applicant files this Response within three months of the 10 March 2006 Office Action and with a number of claims less than or equal to those claims previously paid for. Accordingly, Applicant believes that no extension or claims fees are due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507.

VI. Conclusion

This *Response to Office Action* is believed to be a complete response to the non-final 10 March 2006 *Office Action*. Applicant respectfully asserts that Claims 1-20 are in condition for allowance and respectfully requests passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Hunter Yancey at (404) 885-3696 is respectfully requested.

Respectfully submitted,
TROUTMAN SANDERS LLP

/jameshuntyanceyjr53809/
James Hunt "Hunter" Yancey, Jr.
USPTO Registration No. 53,809
Attorney for INTEL CORPORATION

TROUTMAN SANDERS LLP
Bank of America Plaza
600 Peachtree Street, NE
Suite 5200
Atlanta, Georgia 30308-2216
United States of America
P: (404) 885-3696
F: (404) 962-6828
E: hunter.yancey@troutmansanders.com

DATE: 12 JUNE 2006